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LETTER TO THE EDITOR

The bias-temperature effect in a rectifying Nb/C_{60}/p-Si structure: evidence for mobile negative charges in the solid C_{60} film

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Abstract. Solid C_{60} film was grown on a p-type Si substrate and a rectifying Nb/C_{60}/p-Si structure was prepared. Capacitance–voltage (C–V) measurements showed that for temperatures above 260 K the C–V curve of the Nb/Co_{60}/p-Si structure shifted along the voltage axis depending on biasing conditions. We analysed this effect to reveal the existence of mobile negative charges in the C_{60} layer and determine the density of the mobile charges.

Advances in preparation of abundant quantities of fullerene C_{60} [1] has stimulated a great deal of experimental work on solid C_{60} films [2–12]. Thermal sublimation of purified C_{60} powder in ultra-high-vacuum conditions (UHV) has been a popular method for the C_{60} film growth. By use of this method we have grown solid C_{60} films on crystalline Si substrates and found that an Nb/C_{60}/p-Si structure exhibited rectifying properties due to a heterojunction formation at the interface of solid C_{60} film and p-type Si substrate [12]. This enabled us to study the C_{60} film properties by capacitance measurements of the Nb/C_{60}/p-Si structure under reverse-bias conditions. In this letter we report an important bias-temperature effect on the capacitance of the Nb/C_{60}/p-Si structure. Our results provide the first evidence for the existence of mobile negative charges in conventionally prepared C_{60} film.

Crystalline Si(111) wafers of 40 Ω cm resistivity were polished on the front for C_{60} film deposition. A good ohmic contact to the back of the Si wafer was achieved by a thin Al film deposition followed by a 30 min annealing at 500 °C in an N_2 atmosphere. The Si wafers were dipped in an aqueous 5% HF solution immediately prior to being loaded into the UHV chamber, in order to strip off any surface oxide from the substrate. Source C_{60} powder was prepared by the conventional AC arc method and purified by repeated liquid chromatography to achieve C_{60} purity of 99.9%. Evaporation of the C_{60} powder was performed in a Balzers UMS-500 UHV system with a chamber pressure of 10^{-9} Torr and an Si substrate temperature of 200 °C. The deposition rate was ~ 1 nm min^{-1} and the C_{60} film thickness was monitored *in situ* by a quartz-crystal oscillator. Finally, Nb electrode dots of 5.03×10^{-3} cm^2 area were evaporated on the C_{60} film in the same UHV system. The final thickness of the C_{60} film was determined by use of a surface profiler (Sloan: Dektak 3030 ST). Current–voltage (I–V) measurements revealed that the Nb/C_{60}/p-Si structure was strongly rectifying. As is shown in figure 1, the rectification ratio is greater than 10^4 at ± 2 V. Since we found that an Nb/C_{60}/Nb structure was not rectifying but conducting with linear I–V characteristics [12], which indicated zero or very little potential barrier at the

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Nb/C_{60} interface, the observed current rectification in the Nb/C_{60}/p-Si structure must be due to a potential barrier at the C_{60}/p-Si interface. Thus a heterojunction of solid C_{60} and p-Si is formed. Such a junction is forwardly conducting when the Al electrode on the Si side is positively biased with respect to the Nb electrode on the C_{60} side. A schematic energy diagram of the C_{60}/p-Si heterojunction is shown in the inset of figure 1 where we assume, in agreement with previous reports [8, 9], that the solid C_{60} is a weak n-type semiconductor.

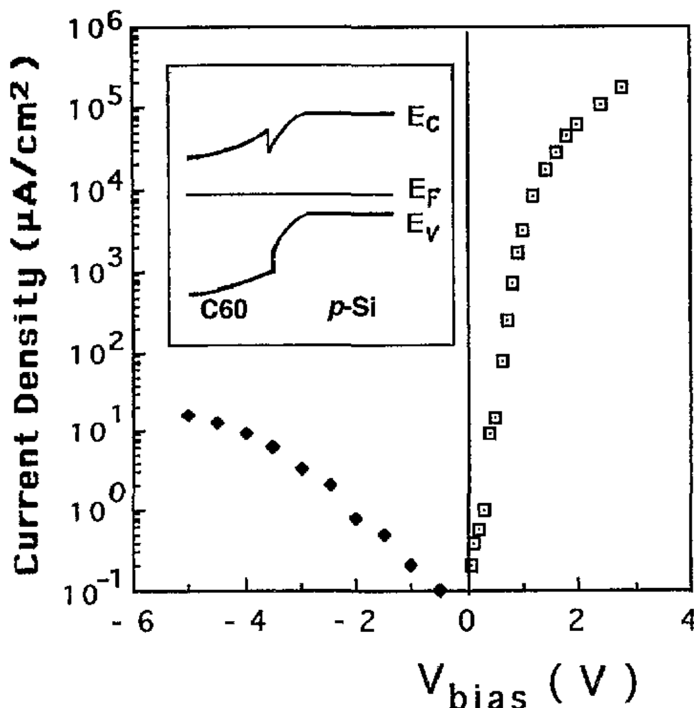

Figure 1. Room-temperature current–voltage characteristics of an Nb/C_{60}/p-Si sample. The inset shows a schematic energy-band diagram of the C_{60}/p-Si heterojunction under thermal equilibrium. V_{bias} is the bias voltage applied to the Si side with respect to the C_{60} side.

Capacitance–voltage (C–V) measurements were performed with a high-frequency (1 MHz) Model 410 C–V plotter. We found that when a slow scan rate (2 V s^{-1}) was used for the ramp voltage of bias, the forward and backward traces of the C–V plot did not coincide. To investigate this phenomenon we performed bias-temperature (BT) experiments, i.e. keeping the sample forward biased or reverse biased for 10 min at a selected temperature and then recording its C–V curve using a fast scan rate (20 V s^{-1}). The results are shown in figure 2 for $T = 360$ K. The curve (a) in figure 2 was obtained before making BT treatments, and the curve (b) was obtained after the sample had been forward biased with $V_{bias} = 3.0$ V for 10 min, while the curve (c) was obtained after the sample had been reverse biased with $V_{bias} = -40$ V for 10 min. The dashed part of the C–V curve in figure 2 indicates that it was plotted under forward biasing and should therefore be corrected to account for forward conduction. It can be seen that curve (b) is shifted to the right while curve (c) is shifted to the left with respect to curve (a) along the voltage axis. Such an effect was found to be saturated at $T \geqslant 350$ K when the shift was stable and at a maximum. The lower the

BT temperature below 350 K, the smaller the shift, and no shift could be observed below 260 K. We have made cycling experiments of the forward and reverse biasing treatments and found that the C–V curve shift was completely reversible, so the aging effect can be ruled out.

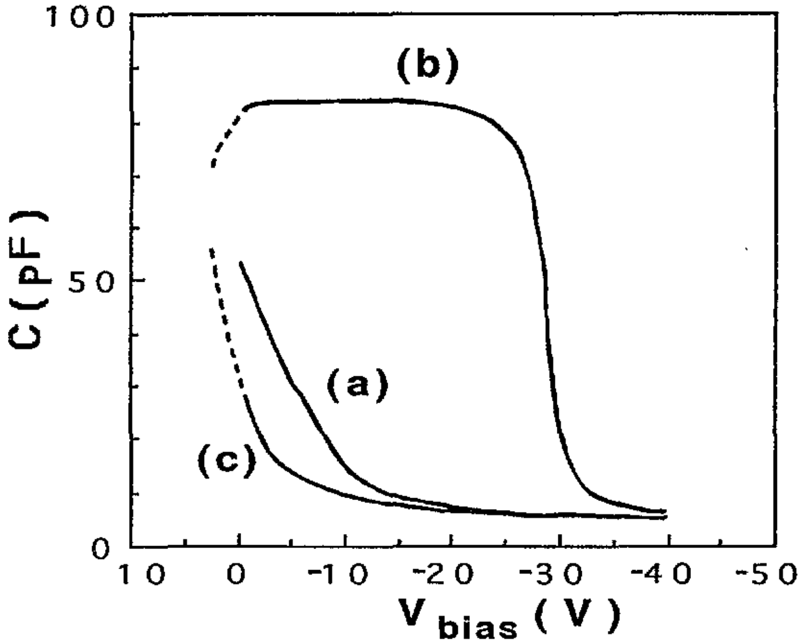

Figure 2. The 1 MHz capacitance–voltage plot of an Nb/C_{60}/p-Si sample at 360 K: (a) before any biasing treatments; (b) after forward biasing treatment with $V_{bias} = 3$ V for 10 min; (c) after reverse biasing treatment with $V_{bias} = -40$ V for 10 min. The dashed part indicates measurements under forward biasing.

In the following analysis, all the capacitance quantities are those of differential capacitance since we have measured the capacitance of the Nb/C_{60}/p-Si structure with a 1 MHz signal. The total capacitance of the Nb/C_{60}/p-Si structure can be considered as a series combination of the C_{60} layer capacitance, denoted $C_{C_{60}}$, and the p-Si depletion-layer capacitance, denoted C_{Si}, i.e.,

$$1/C = 1/C_{C_{60}} + 1/C_{Si}. \qquad (1)$$

Because the C_{60} film was undoped and very thin ($\simeq 200$ nm) the whole layer of C_{60} must be depleted due to the built-in potential of the C_{60}/p-Si heterojuntion. $C_{C_{60}}$ is then given by

$$C_{C_{60}} = A\epsilon_{C_{60}}\epsilon_0/d_{C_{60}} \qquad (2)$$

where A is the Nb electrode area, $\epsilon_{C_{60}}$ and $d_{C_{60}}$ are the dielectric constant and thickness of the C_{60} layer respectively, and ϵ_0 is the permittivity in vacuum. Thus $C_{C_{60}}$ should remain constant and correspond to the maximum total capacitance of the Nb/C_{60}/p-Si system as given by equation (1). As the C_{60} layer is depleted, the Nb/C_{60}/p-Si structure is similar to a metal–insulator–semiconductor (MIS) structure and its C–V data can be analysed similarly

to the data for an MIS structure [13]. The plateau part of curve (b) of figure 2 indicates that the total capacitance remains constant at 8.30 pF for $V_{bias} \simeq 0$–-23 V (V_{bias} is the bias voltage applied to the Si side with respect to the C_{60} side). This can be explained only by an accumulation of holes at the p-Si surface: at the accumulation condition, C_{Si} is much larger than $C_{C_{60}}$ thus the total capacitance is almost equal to $C_{C_{60}}$. Thus we get $C_{C_{60}} = 83.0$ pF for the sample used to obtain figure 2. Because the values of A and $d_{C_{60}}$ are known we can determine the value of $\epsilon_{C_{60}}$ by use of equation (2). We get $\epsilon_{C_{60}} = 3.7 \pm 0.1$, which is in good agreement with a reported value of 3.61 from an ellipsometric study of solid C_{60} film [4], but somewhat lower than two reported values of 4.4 and 4.6 from a low-frequency capacitance study of Al/C_{60}/Al structures [3] and an electron-energy-loss spectroscopy study of small crystals of C_{60} [6], respectively. For $V_{bias} \simeq -28$–-40 V, there is a drop in curve (b) which means that C_{Si} decreases with increasing reverse bias. This can be explained as due to a depletion of holes in the Si surface layer: as the reverse-bias voltage increases, the Si depletion-layer width increases; thus C_{Si} and, subsequently, C decrease.

The accumulation of holes at the Si surface can be caused by negative charges in the C_{60} layer or at the C_{60}/Si interface. If we assume the existence of mobile negative charges in the C_{60} layer the BT effect can be interpreted as follows: the negative charges in the C_{60} layer are forced to move towards the C_{60}/p-Si interface during forward biasing treatment. This leads to an increase in the absolute value of the effective charge density (per unit area), denoted $Q_{C_{60}}$, at the C_{60}/Si interface:

$$Q_{C_{60}} = \left(\int_0^{d_{C_{60}}} x \rho_{C_{60}}(x)\,\mathrm{d}x \right) \Big/ d_{C_{60}} \qquad (3)$$

where $\rho_{C_{60}}(x)$ is the volume charge density in the C_{60} layer. More negative $Q_{C_{60}}$ causes the C–V curve to shift to more positive bias voltage, similarly to the case for an MIS structure [13]. In contrast to the above case, a reverse biasing treatment causes negative charge drift towards the Nb electrode, which results in a less negative $Q_{C_{60}}$, and a C–V curve shift of opposite direction to that in the case of forward biasing treatment. To describe the C–V curve shift we introduce a flat-band voltage at which the Si surface band is flat. The total capacitance at flat-band voltage can be calcualted from [13]

$$1/C_{FB} = 1/C_{C_{60}} + L_D/A\epsilon_{Si}\epsilon_0 \qquad (4)$$

and

$$L_D = (kT\epsilon_{Si}\epsilon_0/p_0 q^2)^{1/2} \qquad (5)$$

where L_D is Debye's screening length, ϵ_{Si} is the permittivity of Si, p_0 is the equilibrium density of holes in the bulk of p-Si, k is Boltzmann's constant, and q is the electronic charge. We get $C_{FB} = 56.2$ pF for the sample giving figure 2. It can be found in figure 2 that the flat-band voltage is -28.0 V for curve (b) while it is 2.5 V for curve (c). The flat-band voltage V_{FB} can be expressed as [13]

$$V_{FB} = -(Q_{C_{60}} + Q_{it})A/C_{C_{60}} + \phi_{C_{60}/Si} \qquad (6)$$

where Q_{it} is the trapped charge density (per unit area) at the C_{60}/Si interface, and $\phi_{C_{60}/Si}$ is the work-function difference between the C_{60} film and p-type Si. The V_{FB} difference, $\Delta V_{FB} = V_{FB}^{(b)} - V_{FB}^{(c)}$, is due to the change in $Q_{C_{60}}$ in the BT experiments, and is given by

$$\Delta V_{FB} = -\Delta Q_{C_{60}} A/C_{C_{60}}. \qquad (7)$$

With $\Delta V_{FB} = 30.5$ V, $C_{C_{60}} = 83.0$ pF, and $A = 5.03 \times 10^{-3}$ cm^2 we get $\Delta Q_{C_{60}} = -3.1 \times 10^{12} q$ cm^{-2}. This corresponds to a volume density of $1.5 \times 10^{17} q$ cm^{-3} for a uniform distribution of the negative charges in the C_{60} layer of 200 nm thickness. Similar analysis for the temperature range of 250–370 K gives a temperature dependence of $\Delta Q_{C_{60}}$ as shown in figure 3. It can be seen that the higher the biasing temperature, the larger the value of $|\Delta Q_{C_{60}}|$. For temperatures above 350 K, $|\Delta Q_{C_{60}}|$ reaches the maximum value and remains constant which means that the BT effect is saturated.

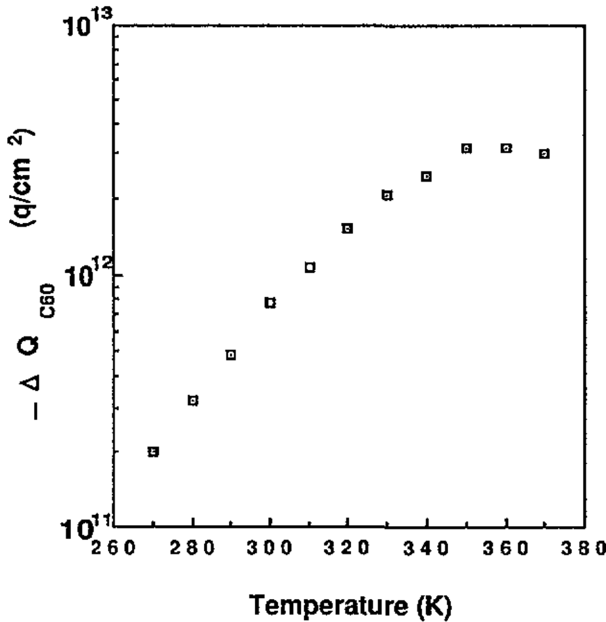

Figure 3. The effective density of mobile negative charges per unit area versus the temperature of the biasing treatment.

The origin of the negative charges giving rise to the BT effect remains to be investigated. It is well known that the solid C_{60} lattice presents a fairly open structure. It is face-centred cubic at room temperature with a lattice constant of 14 Å and the C_{60} nearest distance of 10 Å (the C_{60} radius is 3.5 Å). Such material can contain solvent molecules or atmospheric contaminants in the large interstices within the C_{60} lattice. A recent work by Chen *et al* [10] has reported that a large amount of helium can be intercalated in the solid C_{60} lattice and that the helium must be mobile within the lattice. However, no information about the charge state of the helium in the solid C_{60} has been given. In our samples of the Nb/C_{60}/p-Si structure the C_{60} film was grown by sublimation of C_{60} powder which was prepared by the conventional AC arc method under a helium atmosphere. Helium contamination in our samples cannot be ruled out. Furthermore, our samples were exposed to air for several days before and during the measurements. Therefore, other contaminations such as oxygen might contribute to the origin of the mobile charges in the C_{60} layer. Finally, we note that Pichler *et al* [11] have proposed the existence of extrinsic charge carriers to explain the dark conductivity in the solid C_{60} film. They prepared the solid C_{60} film by use of the sublimation method with a source C_{60} purity of 99.9%, the same technique as used for our film preparation.

In conclusion, we have observed a strong effect of the bias-temperature treatment on the high-frequency capacitance of the Nb/C_{60}/p-Si structure and attributed this effect to the existence of mobile negative charges in the C_{60} layer. This work also demonstrates that capacitance measurements on the heterojunction of solid C_{60} and p-type Si can be applied for monitoring contaminations in the solid C_{60} film.

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